WHAT IS CLAIMED IS:

1. A semiconductor device comprising a plurality of alignment marks formed over a semiconductor wafer,

each of the alignment marks being divided by a micronized pattern.

2. A semiconductor device according to claim 1, wherein

the micronized pattern is a line-and-space pattern.

3. A semiconductor device according to claim 2, wherein

lines of the line-and-space pattern are divided by a required length.

4. A semiconductor device according to claim 3, wherein

positions of the divisions of the lines are offset from those of the divisions of their adjacent lines.

5. A semiconductor device according to claim 1, wherein

a margin for forming the micronized pattern to be formed in is larger than a margin for a device pattern to be formed on the semiconductor wafer.

6. A semiconductor device according to claim 2, wherein

a margin for forming the micronized pattern to be formed in is larger than a margin for a device pattern to be formed on the semiconductor wafer.

7. A semiconductor device according to claim 3, wherein

a margin for forming the micronized pattern to be formed in is larger than a margin for a device pattern to be formed on the semiconductor wafer.

8. A semiconductor device according to claim 4, wherein

a margin for forming the micronized pattern to be formed in is larger than a margin for a device pattern to be formed on the semiconductor wafer.

9. An alignment sensing method for a semiconductor device, in which illumination is applied to alignment marks formed on a semiconductor wafer with a device pattern, reflected light or diffracted light of the illumination on the alignment marks is formed into images, and based on image signals obtained by processing the formed images, alignment of the device pattern is sensed,

each of the alignment marks being divided by a micronized pattern, and

a resolution for forming images of the reflected light or the diffracted light of the illumination on the alignment marks being made capable of discriminating the alignment marks but incapable of discriminating the micronized pattern.

10. An alignment sensing method for a semiconductor device according to claim 9, wherein

the micronized pattern is a line-and-space pattern.

11. An alignment sensing method for a semiconductor device according to claim 10, wherein

the lines of the line-and-space pattern are divided by a required length.

12. An alignment sensing method for a semiconductor device according to claim 11, wherein

positions of the divisions of the lines of the line-and-space pattern are offset from those of their adjacent lines.